AUDIO ADC DYNAMIC RANGE MATCHING BY MEANS OF A DSP EQUALIZER AND DYNAMICS PROCESSOR COMBINATION

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ABSTRACT

An ideal analog-to-digital interface should be an universal interface. Different analog devices, spanning from microphones up to HiFi control amplifiers, that vary in lower or higher nominal levels or in different output resistances, should be connected to the universal analog-to-digital interface in a plug-and-play manner. The user then should not be forced to make any necessary adjustments such as setting gain ranges or adjusting input resistances. The analog-to-digital interface consists of analog signal conditioning followed by an analog-to-digital converter. Currently, the available audio analog-to-digital converters are insufficient for these requirements due to a too small dynamic range. An alternative and already known conversion technique, not perfect for all intents and purposes, but highly feasible, is the multi range analog-to-digital converter that combines analog and very precise digital signal processing. The discussion of a particular class of multi range converters is the topic of this paper.

1. SINGLE RANGE AND MULTI RANGE ANALOG-TO-DIGITAL CONVERTERS INTENDED FOR THE USE AS AUDIO CONVERTERS

One of the main challenges in the field of audio signal processing is the very high dynamic range of about 135dB. This number, seen as a highlighted number, approximately corresponds to the mid frequency dynamic range of hearing or to the dynamic range of a high-grade condenser microphone. The junction system between the analog and the digital signals is, at present, the 24-bit audio analog-to-digital converter ADC. Such a 24-bit ADC should theoretically be able to cover this dynamic range completely. But in reality, the ADCs achieve significantly lower values, not exceeding about 125dB. Reviewing the last two decades of audio ADC development, we have seen an impressive increase of nominal resolution from the 16-bit ADC over 18 bit and 20 bit up to the 24-bit ADC and we have seen an also impressive increase of the maximum sampling frequency, ranging from 48kHz over 96kHz up to 192kHz. Even if it seems to be unnecessary, it is possible to buy ADCs offering a maximum sampling frequency of 384kHz. The dynamic range increased steadily too but not in the same manner. We can dare the prognosis that the dynamic range will not reach the above mentioned value of 135dB or even more for the next years.

An universal analog-to-digital interface is a system-in-a-box and should not only cover the whole dynamic range but it also should be used without the necessity of adjustment procedures that make sure the proper operation. Such an interface would make believe the user that the digital audio output signal is a generic 24-bit digital signal and would at no time have been an analog audio signal.

The reason for a restricted dynamic range of an audio ADC is the converter noise that is mainly the modulator noise. To overcome this restriction, a typical single range ADC will be combined with an analog amplifier in front. Fig.1 shows this arrangement where the analog amplifier gain can be set by the user, often in a number of steps. This works satisfactorily if we imply that the amplifier noise level is significantly lower than the ADC noise level and if the source dynamic range does not exceed the ADC dynamic range and if the source dynamic range is a slidable part (sliding by altering analog gain) of the amplifier extended dynamic range. The user of such a typical single range system must set the gain accordingly to the electrically connected analog device. We assume that the occurrences of gain settings are infrequent, perhaps only in the case of exchanging the microphone or in the case of micing an acoustic guitar now and close up micing the drums later.

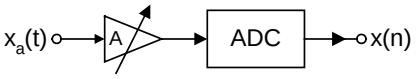

Figure 1: *ADC with adjustable analog gain*

The objective of this paper is to point to the multi range ADCs that have been proposed some years ago for electronic balances [1], realized with an single ADC and two analog amplifiers of different gains that are alternatively switched to the ADC where the switching activity was controlled by a digital signal processing device, or multi range ADCs for video systems [2], and, last but not least, multi range ADCs for audio systems [3,4,5]. The common principle of these converters is the splitting of the signal processing into two or more branches of different analog signal gain factors accessing similar ADCs. Multi range ADCs are currently the only available converters of acceptable costs with which universal analog-to-digital interfaces can be constructed. Despite of this affirmatory statement we should not forget, that multi range ADCs are not ”as-well-as-converters“ but rather ”either-or-converters“ [6] that cannot convert simultaneously two signals, sine waves for example, with magnitudes at the upper and at the lower end of the specified dynamic range, since the lower level signal will perish in the converter noise.

But, due to the masking properties of hearing this problem can be of lower significance in practice.

We will introduce a useful point of view on multi range audio ADCs offering an extended dynamic range that helps on the one hand to better comprehend the working principles and the strict requirements of the analog and of the digital signal processing and, on the other hand, it refers to the well known and extensively documented techniques of audio dynamic processors [7]. The necessary signal equalization will be seen as a task of statistical signal processing where typical methods can be applied in consequence. So, not only appropriate estimators and their specific DSP implementation will be proposed but also the effects of the estimators on the dynamic range of multi range ADCs will be analyzed. To give an idea of the implementation, we will discuss a dual range ADC that reaches a sufficient large dynamic range at low costs. The reader will learn about some aspects of the implementation that are of particular significance.

2. SIGNAL BRANCHES OF MULTI RANGE ADCS

A multi range ADC in Fig. 2 is based on multiple signal branches of constant but differing and staggered analog gains and multiple ADCs, one ADC as part of each of the branches. Selecting the active branch, which means selecting the appropriate gain, is done by a digital signal processing unit, that can be implemented on a DSP, for example. The active branch is always the branch of the highest signal to noise ratio.

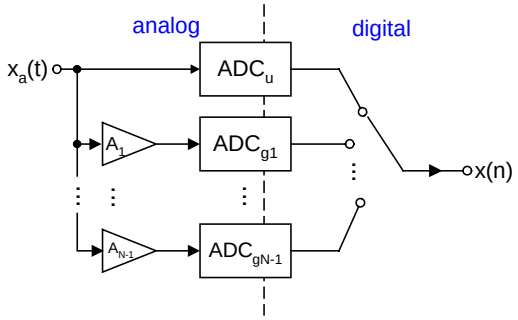

Figure 2: *Multi range ADC with analog and digital signal processing*

The N signal branches are denoted by u, g_1, g_2, ..., g_{N-1}, where u refers to the signal branch of the largest signal level range or to the lowest branch gain factor, respectively. The signal branch g_{N-1} refers to the branch of the lowest signal level range or to the highest branch gain factor, respectively. In the particular case N=2 we denote the two branches by u and g. The branch gains $G_u<G_{g1}<G_{g2}<...<G_{g(N-1)}$ increase according to the increasing branch index. In order to simplify the presentation, we normalize all branch gain factors by the lowest branch gain factor, the branch u gain factor. Then the branch u gain is set to G_u=0dB. Fig. 3 shows exemplary the dynamic ranges of a N=3 branches multi range ADC. What is the benefit of a multi range ADC? The gain switching can be executed automatically without user interaction. Also in case of a multi range ADC we can assume that gain range switching occurs relatively seldom. Thus it can then be said that the user employs an analog-to-digital interface without manual control elements.

Such an analog-to-digital interface can be designed to be an universal interface that works likewise at the low levels of dynamic microphones, at the higher levels of condenser microphones or even at the typical high line levels of tape recorders or control amplifiers. An outstanding multi range ADC system with N=4 is produced by Stage Tec and is denoted by ”TrueMatch“ [4]. The Stage Tec converter gains are G_u=0dB, G_{g1}=20dB, G_{g2}=40dB and G_{g3}=60dB.

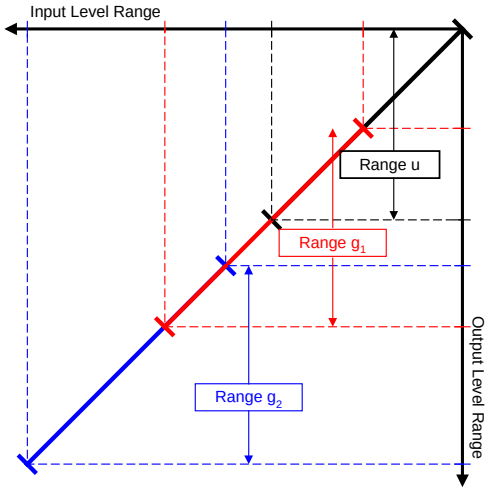

Figure 3: *Overlapping dynamic ranges of a N=3 multi range ADC*

Making the decision on implementing a small number of ranges, at least N=2, or on implementing a larger number of ranges, N=4 or even more, has two far-reaching impacts. A large number N multi range ADC requires complex electronic circuitry and gain switchings appear at a higher frequency which seems to be a severe drawback. On the other hand, a very high dynamic range can be obtained and the digital signal processing will be simplified considerably in terms of the precision requirements. To be precise, an obtainable high dynamic range is not only the result of a large difference in the branch gains G_u and $G_{g(N-1)}$, even 60dB at the Stage Tec converter, but also it is a result of consequently relative small gain differences between two consecutive branches. However, we can set the gain difference of G_u and G_g to large values in case of N=2 too, provided, the ADCs are of sufficient quality. But, then the inevitable large differences between the branch signal characteristics are more hardly to handle than in the case of a N>2 multi range ADC.

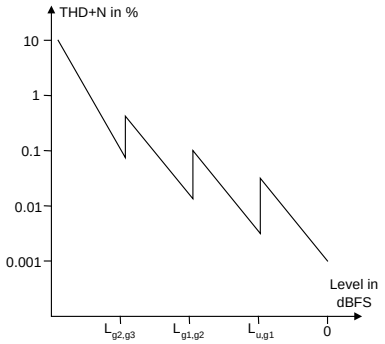

Figure 4: *THD+N characteristic of a N=4 multi range ADC*

An extension of the dynamic range can not increase limitless by means of an increasing number of branches due to an inherent lower limit that is determined by the amplifier noise of the maximum gain branch. Fig. 4 shows clearly the principal characteristics of the THD+N distortion measure of a N=4 multi range ADC versus the level of the digital signal. The level values $L_{u,g1}$, $L_{g1,g2}$ and $L_{g2,g3}$ are the threshold levels of the branches ordered in consecutive pairs. We recognize two determining factors. The THD+N value increases corresponding to decreasing signal levels and decreases, if the system switches to branches of higher gain. The underlying upward trend of the THD+N curve is caused by the above mentioned analog amplifier noise. Zooming to a single branch one recognizes increasing THD+N numbers due to the ADC noise which is independent on the signal level. With respect to this noise, the threshold levels should be chosen as large as possible but increasing distortions due to high level signals must be avoided by choosing this level low enough. In practice, the values are determined not only based on calculations but also based on careful measurements that acquire the THD-N measure over the signal level.

3. DIGITAL SIGNAL PROCESSING AT MULTI RANGE ADCS: EQUALIZER AND DYNAMICS PROCESSOR

It is helpful to split the digital signal processing section of a multi range ADC into two separable units. The first unit is an auxiliary unit that equalizes the signals after having passed the analog signal amplifiers and the ADCs. This pairwise equalizing is necessary in order to increase the precision of the signals with respect to offset and gain up to the level of a digital signal processing in order to enable the suppression of glitches and of modulation noise due to gain factor switching. This unit will be referred in the following to as *equalizer*. The second unit is a *dynamics processor* that performs the dynamic range switching. So we speak about carrying out two digital signal processing tasks:

- modeling of the analog signal processing section and using the model for the design of the equalizer,
- adapting an audio dynamics processor to the signal level controlled digital gain stage.

A dynamics processor, shown in Fig. 5, is a nonlinear signal processing device which will be implemented either in the configuration *feed-forward* or in the configuration *feed-back*, depending on the place where the signal level will be detected, input signal or output signal, respectively. This signal level, compared with a reference level, controls the system gain or the signal switch (stepped gain element), respectively. Since digital signal processing enables the delay of signals without loss of quality, the feed-forward dynamics processor will be preferred. So, some induced nonlinear signal distortions can be reduced by applying appropriate signal delay.

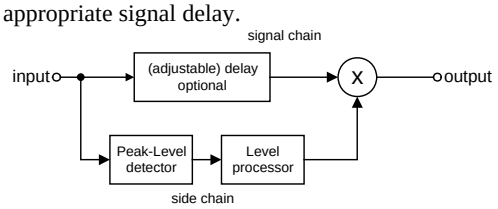

Figure 5: *Standard dynamics processor*

4. ENVELOPE-MODE AND SYLLABIC-MODE

The dynamics processor can operate in two modes, an *envelope-mode* with signal delay and a so called *syllabic-mode* without signal delay. In the envelope-mode, the gain switching follows the envelope of the signal. Switching from a higher gain branch to a lower gain branch is made less ”nervously“ by an *attack time* in the envelope-mode. Overload distortions must be avoided by applying a signal delay according to this attack time. Switching back from a lower gain branch to a higher gain branch is delayed by a *release time* in the envelope-mode.

The syllabic-mode has to be chosen if a signal delay can not be accepted. Switching from a higher gain branch to a lower gain branch occurs instantaneously. Switching back from a lower gain branch to a higher gain branch is delayed by a fixed minimum hold time of 100ms to 300ms. This time span corresponds approximately to the time span in which syllables will be spoken.

5. THE EXAMPLE OF A N=2 DUAL RANGE ADC

In the following we will discuss in detail the realization of a N=2 dual range ADC whose digital signal processing sections consists of an equalizer and a dynamics processor as it is shown in Fig. 6. We have chosen a dual range ADC since the present 24 bit audio ADCs are of considerable high quality, enabling the development of a low cost and low space system what have been the primary design goals. The use of lower quality ADCs would require a greater number N of ranges. Fig. 7 shows the analog signal processing section consisting of the four amplifiers A_1, A_2, A_{3u} and A_{3g}. The amplifier A_1 is an impedance converter that can be omitted in the case of operating the dual range ADC as microphone interface only. The amplifier A_2 is a special amplifier combined with an elaborate soft limiting stage that suppresses nonlinear distortions at the amplifier input due to overloading. It must be considered that distortions at this place will be also amplified by the amplifier A_{3g}. Overloading the amplifier A_2 occurs necessarily in a dual range ADC. Hints and circuit examples for the design of two similar elaborate limiting stages are given in [8] and in the data sheet of the operational amplifier OPA627 [9]. The amplifiers A_{3u} and A_{3g} are the driver amplifiers of both ADCs. They provide both the necessary low impedance driving signals and the common-mode voltage of the ADC at the driver amplifier output terminals.

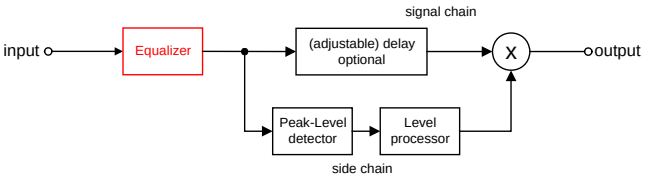

Figure 6: *Dynamics processor and equalizer*

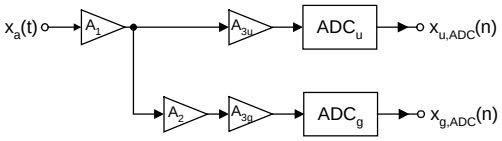

Figure 7: *Analog signal processing section of a N=2 dual range ADC*

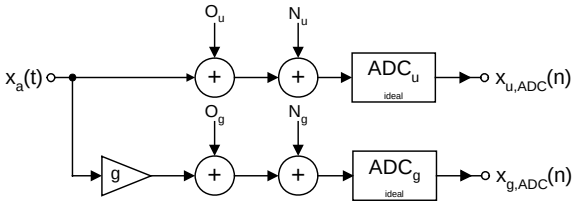

Figure 8: *Linear model of the analog signal processing section of a N=2 dual range ADC*

6. DESIGN AND ALGORITHMS OF THE EQUALIZER STAGE

It is well known that a stepped gain adjustment causes often clicks if gain changes occur. In case of a standard single range converter in Fig. 1 the clicks can mostly be accepted, since changes of the gain occur rarely and are "expected" by the user, for example, if a microphone is replaced by another microphone of different sensitivity. In case of a multi range ADC where gain switching occurs depending on the actual level of the signal, clicks cannot be accepted. So, the design must include a careful consideration of discontinuities of the branch signals at the moments of switching, even if these moments occur relatively rarely (due to a small number of branches, for instance). These discontinuities must be compensated or, at least, temporarily masked in the case of noise level differences.

The equalizer has no signal processing function and could be omitted if it would be possible to implement analog signal processing as precisely as digital signal processing can be implemented. The precision of analog signal processing depends on temperature drift, tolerances of the components and noise characteristics of amplifiers and ADCs. The function of the equalizer is the equalization of the differences belonging to the analog to digital converted branch signals. Even if the nominal gains are known, one has to consider significant and time depending differences that can be made lower by a larger number of branches. In order to show the necessity and the properties of the equalizer, a simple linear model of the analog signal processing section, including the ADCs, is presented in Fig. 8. The model consists of a gain stage and of additive error signals that are caused by different mechanisms. The offset values O_u and O_g are most often slowly drifting signals that can be eliminated by linear digital signal processing methods like high pass filtering, for instance. The amplifier and ADC noise signals N_u and N_g, and the even more problematic differences of the noise signal levels in the branches that cause molesting noise modulations cannot be eliminated by signal processing. But they can be masked in order to get a subjective (psychoacoustical) improvement. As larger as N, the number of ranges, will be chosen, as lower are the noise level differences between two consecutive branches. This is a strong argument for implementing more than two branches. The intention of noise masking is the elimination of the noise level discontinuities in Fig. 9 by replacing the discontinuities with additive noise, corresponding to the dotted lines in the figure. The masking noise then depends on the level of the wanted signal and on the difference of the noise levels in the proximity of the switching level thresholds. An alternative to this kind of noise masking is the addition of a cross fading which makes the signal equalizing significantly less critically.

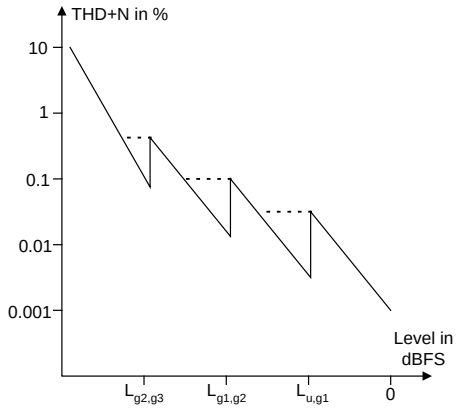

Figure 9: *THD+N characteristic of a N=4 multi range ADC with noise difference masking (dotted lines)*

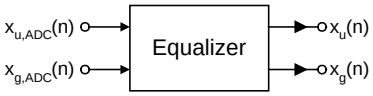

Figure 10: *N=2 dual range ADC equalizer*

The equalizer in Fig. 10 is a MIMO-system consisting of N inputs and N outputs. It has to be designed without signal delays. Fig. 11 shows the block diagram of a N=2 equalizer.

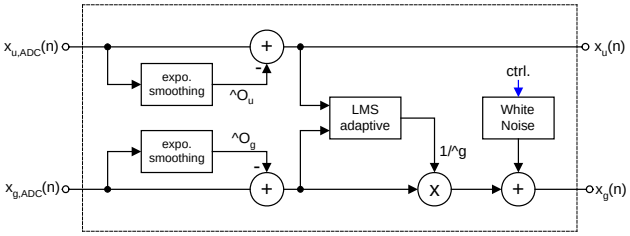

Figure 11**:** *N=2 dual range ADC equalizer signal processing*

The equalizer has to perform three tasks:

- **Removing the signal offsets O_u and O_g in the branches u and g (DC signal components)** It should be noted that if the signal offsets are removed digitally, the analog amplifiers can be DC coupled amplifiers without adding the otherwise necessary circuitry like DC servo amplifiers or offset

voltage trim potentiometers. The DC signal components correspond to the expectation values $E\{x_u\}$ and $E\{x_g\}$ of the audio signals. There exist several methods to acquire these expectation values that have to be subtracted from the audio signals in the consequence. For the reason of simplicity we have chosen simple exponential smoothing. Exponential smoothing with a small smoothing factor α yields a strong suppression of signal variance corresponding to $\sigma^2_y/\sigma^2_x=\alpha/(2-\alpha)$ (we can also speak about a small equivalent noise or audio bandwidth, respectively). Implementing exponential smoothing on a 24-Bit fixed point DSP, we use DSPs of the Freescale DSP563xx family, should preferably be done as it is shown in Fig. 12, using a single multiplication and two additions.

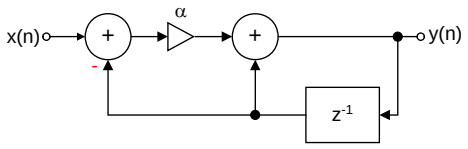

Figure 12: *Exponential smoothing*

- **Estimation of the reciprocal gain factor** The reciprocal gain factor is necessary to bring the two free of offset branch signals to the same level so that switching can be done without clicks. There exist also several methods. Before presenting the method referred to in this paper, it should be given an analysis of the task. The analysis is based on signal and noise powers and on the gain factor ratio of the two branches u and g. We introduce
  - r: nominal gain factor ratio of the two branches u and g and ρ is an estimated value of r,
  - P_u, P_g: Powers of the (wanted) signals in the branches u and g that are related by $P_g = r^2 P_u$,
  - $P_{N,ADC}$: Power of ADC noise, equal valued in both branches and including the common amplifier noise power,
  - $P_{N,g}$: Power of the exclusive amplifier noise in branch g with $P_{N,g} < P_{N,ADC}$. ADC noise and amplifier noise are assumed to be uncorrelated. The functional principle of dual range ADCs is based on this difference of noise powers.

We assume that the signal-to-noise-ratios snr_u and snr_g of both branches are different and that their values are interrelated by the inequality

$$snr_u = P_u / P_{N,ADC} < P_g / (P_{N,ADC} + P_{N,g}) = r^2 P_u / (P_{N,ADC} + P_{N,g}) = snr_g . \quad (1)$$

There exist several estimators yielding an estimated value ρ^{-1} of the desired reciprocal gain factor r^{-1}. We focus on the two most widely known estimators based on the expectation values of the rectified signals $E\{|x_u|\}$ and $E\{|x_g|\}$ and on the expectation value of the signal product $E\{|x_u|\,|x_g|\}$, reading

$$S_1: \rho_1^{-1} = \{E\{|x_u|\,|x_g|\}/E\{|x_g|^2\}\} \quad (2)$$

and

$$S_2: \rho_2^{-1} = \{E\{|x_u|^2\}/E\{|x_u|\,|x_g|\}\}. \quad (3)$$

These estimators minimize the expectation values of the estimation errors $e_1(1/\rho)$ and $e_2(1/\rho)$, respectively, with

$$S_1: E\{e_1(1/\rho)\} = E\{ (|x_u| - (1/\rho)\,|x_g|)^2 \} \quad (4)$$

and

$$S_2: E\{e_2(1/\rho)\} = E\{ (\rho\,|x_u| - |x_g|)^2 \}. \quad (5)$$

Both estimators are biased. The bias of estimator S_1 is

$$S_1: \rho_1^{-1} = r^{-1}\,(snr_g/(1+ snr_g)) \text{ leading to } \rho_1^{-1} \leq r^{-1}. \quad (6)$$

This estimator underestimates the desired value. The degree of underestimation increases in compliance with a decreasing signal to noise ratio snr_g. The ratio snr_g decreases with decreasing signal power or decreasing excitation, respectively. If the estimated value decreases due to decreasing excitation, then we attain a desirable effect of dynamic expansion at lower level signals. Furthermore, we observe in expression (6) that the estimator S_1 is appropriate if the branch u noise exceeds the branch g noise which is true for this application. The bias of estimator S_2 is

$$S_2: \rho_2^{-1} = r^{-1}\,((1+ snr_u)/ snr_u) \text{ leading to } \rho_2^{-1} \geq r^{-1}. \quad (7)$$

This estimator overestimates the desired value. The degree of overestimation increases in compliance with a decreasing signal to noise ratio snr_g. If the estimated value increases due to decreasing excitation, then we get an undesirable effect of dynamic compression at lower level signals.

Computing ρ_1^{-1} in (2) requires a large amount of state memory for the averaging and also a division operation which makes this estimator unattractive for a DSP application. Instead, we propose the use of an adaptive linear LMS method that minimizes the estimation error $e_1(1/\rho)$ of S_1 in (4). The adaptive system requires no division and it will be driven with the rectified signals $|x_u(n)|$ and $|x_g(n)|$. The difference equation of the updating rule reads as

$$(1/\rho(n)) = (1/\rho(n-1)) - 2\mu\,(1/\rho(n-1))\,|x_g(n-1)|^2 + 2\mu\,|x_g(n-1)|\,|x_u(n-1)|, \quad (8)$$

where μ is a step size factor gaining the steps in the descent direction. This adaptive estimator can be implemented with only four multiplications and two additions. Using the DSP `mac`-operation, only five arithmetical operations are necessary. It should be noted that this LMS adaptation algorithm is not normalized which, in consequence of, leads to increased adaptation times with respect to decreasing signal levels. So, the adaptation should work preferably at higher signal levels and should be interrupted, if the signal level undergoes an appropriate threshold.

The rectified signals are the output signals of ballistic peak value rectifiers with attack time and release time characteristics. Such rectifiers, designed as simple nonlinear systems, have been proposed and discussed in [7]. For this application actually, effective value rectifiers, computing the expectation values of the squared signals, should be preferred. But since both signals differ ideally by a (quasi) constant factor only and since the peak value rectifiers are bal-

listic rectifiers, we can neglect this argument. The primary reason of choosing a peak value rectifier in the equalizer was the necessity of using a peak value rectifier in the dynamics processor of the multi range ADC in the envelope mode.

- **Masking noise level differences** The switching from a higher gain branch to a lower gain branch is done at the presence of high level signals (high loudness) where we profit by psychoacoustical masking of the noise level step. In contrast, the switching from a lower gain branch to a higher gain branch is done at the presence of low loudness. An audible noise level step then must be masked by the equalizer signal processing. So, the third system is based on a noise generator (24 bit shift register sequence of maximum length period) and produces a modulated white noise signal that is to be used for masking the noise difference of the branches u and g. If the analog amplifiers would be noise less amplifiers, the ratio of both noise powers would be the squared gain. In the praxis, the ratio is lower due to analog amplifier noise. The noise signal is modulated by the rectified signal $|x_u(n)|$. In addition, this modulated noise signal will be exponentially decayed and added to the signal of branch g. So, the noise level reduction due to the transition from branch u to branch g will be masked (subjective improvement). The added noise signal can be written as

$$r(n) = d(n)\,|x_u(n)|\,b\,a^n,\ n\geq 0,\ 0<b<1, \qquad (9)$$

where d(n) denotes the 24 bit noise signal, b denotes a scaling factor and the factor a determines the decay characteristic. The scaling factor b has to be chosen such that the noise level difference between both the signal branches will be reduced [10,11]. The adjustment of this difference noise masking operation in Fig. 9 must be executed by means of measurements. The adjustment procedure is based on adding the temporal constant noise signal

$$r(n) = d(n)\,|x_u|\,b \qquad (10)$$

and executing THD+N monitoring with respect to the relevant level range. The goal is to reach the desired noise levels, marked with dotted lines in Fig. 9. We assume that the frequency of the sinusoidal test signal is large enough that the rectified signal $|x_u(n)| = |x_u|$ in (10) can be seen as a time invariant signal.

The noise masking unit will be triggered (resetting the sample counter n to zero) by the switching transition from branch u to branch g.

7. IMPLEMENTATION OF THE DYNAMICS PROCESSOR

A general dynamics processor consists of two signal branches, the s*ignal chain*, where the (delayed) signal will be amplified or attenuated, respectively, and the s*ide chain*, where, depending on the level of the signal, the instantaneous signal gain factor (or attenuation factor) will be computed.

The function of the dynamics processor as part of a multi range ADC is the signal level depending control of the signal switch with N positions and N-1 signal thresholds. In our case, the case N=2, the side chain detects the level of the branch u signal and derives the control signal of the two positions signal switch. Doing so, we can cover a large range of signal levels, sufficiently above the noise level and sufficiently below the distortion limit level. The dynamics processor will be driven in two modes:

- *Syllabic-mode SM* [10] without delay in the signal chain. A hold stage in the side chain is used to delay the gain increases. Gain decreases occur instantaneously. The reason for using the hold stage is making the switching more rarely. The hold time is most often set to a range of 100ms to 300ms which corresponds to the rate at which syllables vary with speech [11].
- *Envelope-mode LD* with delay in the signal chain and using a ballistic peak value rectifier as level detector in the side chain.

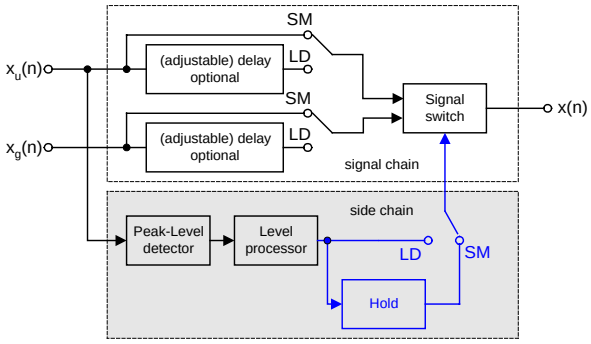

Figure 13: *Dual range ADC dynamics processor*

The dynamics processor in Fig. 13 consists of the following signal processing blocks:

- The *level detector* in Fig. 14 detects the branch u signal level in the case N=2 and utilizes in the envelope-mode the already implemented ballistic peak value rectifier of the equalizer. In the syllabic-mode only a simple absolute value rectifier is used. The branch u rectifier output signal is $|x_u(n)|$.

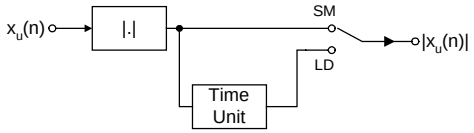

Figure 14: *Level detector*

- The *level processor* is a threshold decision maker applying N-1 thresholds. The decision maker renders the trigger signal of the hold stage in the syllabic-mode and the trigger signal of the signal switch in the envelope-mode, respectively. In the case of N=2, the branch u signal level L_u leads to the decision. In general, the signal levels L_{gk}, k=1,...,N-2, lead to the decisions of switching between the branches g_k and g_{k+1}. The value of the threshold can be chosen with some degree of freedom. We recommend a relatively low value which avoids using the branch g signal at high levels

in order to reduce distortions (for instance ADC filter prerinjging effects near the excitation limit).

- The *hold stage* in the syllabic-mode forces a minimum of time at which branch u is the active branch. The hold stage is not locked and will be retriggered as often as the trigger signal is active during the hold time. The negative edge of the hold stage impulse is used to start the modulated noise generator that is placed in the equalizer.
- The *delay stage* reduces in the envelope-mode the nonlinear signal distortions that are caused by changing the signal gain (look ahead functionality). The time of signal delay should reach at least the attack time of the ballistic peak value rectifier. But for all that it should be noted that some fields of application forbid a significant signal delay that will in addition be increased effectively by the ADC inherent delay. We mention that a signal chain delay also helps to reduce possible distortions due to the ADC filters that can become critical at high levels.
- The N positions *signal switch* switches between the 48 bit wide branch signals that are the two branches u and g signals in the case of N=2. The requantization unit, where the 48 bit signals are requantized to either 24 bit signals or to 16 bit signals, should be equipped with a noise shaper and, in addition, an appropriate dither signal should be applied, in particular for the case of a 16 bit output signal. The noise shaping is realized by psychoacoustical in-band-noise-shaping in case of the sampling frequencies 44.1kHz and 48kHz. In case of higher sampling frequencies we use out-of-band-noise-shapers according to the parametrized noise shaping function of the type $E_p(z)=(1-z^{-1})^p$, for which the parameter value p=4 is a preferred value in terms of decorrelating signal and requantization error on the one hand and the DSP computational effort on the other hand. This out-of-band-noise-shaper can be implemented using the two double precision fixed point DSP operations `shift` and `add` only, since the filter coefficients are integer valued coefficients. An in-band-noise-shaper, in contrast, is implemented with single precision DSP multiplications.

8. PRACTICAL EXAMPLE: AN UNIVERSAL DUAL RANGE AUDIO ANALOG TO DIGITAL INTERFACE

In the following some details of a N=2 dual range ADC are presented. The analog components are an audio ADC of type PCM4222 (Texas Instruments) and audio operational amplifiers of the types LME49990 (National Semiconductors) and OPA1632 (Texas Instruments). The latter operational amplifiers, amplifiers for balanced signal amplification, are the driver amplifiers of the ADC. The digital signal processing is executed with a digital audio signal processor of type DSP56374 (Freescale). The unnormalized branch gains are –14dB in branch u and +30dB in branch g. Operated at a sampling frequency f_T=192kHz, a dynamic range of more than 140dB, a-weighted, was reached. The digital output full scale corresponds to an analog signal level of 22dBu. The corresponding equivalent input noise rms voltage is about 1µV(a-weighted). An exemplary condenser microphone is the Neumann-U87 microphone that is rated by: omnidirectional operation, sensitivity 20mV/Pa and equivalent microphone noise level of 15dB(a). Then the noise level corresponds to an equivalent noise voltage of 2.2µV(a). In combination with the dual range ADC the total noise voltage results in the rms-added value of 2.42µV(a). The digital output is a standard AES3 conform 24 bit output. Two figures, Fig. 15 and Fig. 16, show the FFT signal spectra of a sinusoidal analog input signal at the two output levels of -13dBFS and –103dBFS, corresponding to using the branch u and the branch g, respectively. In Fig. 15 some small residual distortions in branch u can be observed that are injected by the overloaded branch g signal amplifier.

If a better performance is required, in particular for the use as interface for very low sensitivity microphones, then the analog amplifiers must be aligned. This means that the input resistance has to be reduced to the specified microphone minimum load resistance and the first amplifier stage should be constructed by means of very low noise discrete transistors (transistor arrays). A second enhancing technique is increasing the number of branches from N=2 to N=4. However, it should be considered that both techniques are cost intensive and a large number of branches causes frequent gain switching operations.

9. CONCLUSION

An universal Audio ADC interface without user adjustable analog gain requires a dynamic range that exceeds significantly the typical dynamic range of a present 24 bit audio ADC. Multi range ADCs can overcome this dynamic range restriction but there are some conflicting objectives. For instance, a large number of ranges can enable indeed a very high total dynamic range but the consequent high range switching activity causes unwanted signal artifacts.

Digital signal processing is used for the task of signal depending automatic gain control using an equalizer and a simple dynamics processor. In this paper we recognize the analog channel mismatch distortions as statistical signals that have to be processed by methods of statistical signal processing. Estimators of analog signal distortions are proposed and analyzed where an useful effect of increasing the dynamic range at the lower level end could be recognized. Adding some further signal processing such as noise masking and signal delay as parts of a dynamics processor help to reduce the signal distortions that occur in consequence of gain switching. Finally some details of a realized low cost two range ADC are given, showing the high performance of this audio converter topology.

10. REFERENCES

[1] J. Chou, *Dual-range analog-to-digital convertor*, EPO Patent EP 0 278 187 A2

[2] L. Berstein, *High level resolution enhancement for dual-range A/D conversion*, US Patent 5250948, 1993

[3] C. Langen, “Design and Implementation of a Digital Interface for Microphones According to AES42-2001”, M.S. thesis, Karlsruhe University of Applied Sciences, 2001

[4] Stage Tec, Entwicklungsgesellschaft für professionelle Audiotechnik mbH, *True match*, Available at http://www.stagetec.com/ web/de/ audiotechnik-produkte /truematch-rmc/konzept.html

[5] C. Wegner, “Entwicklung und Aufbau eines Audio-AD-Wandlers mit hoher Dynamik”, Diplomarbeit 1994, ITA, Prof. Kuttruff, RWTH Aachen

[6] Prosig, Available at http://blog.prosig.com/2010/11/18/high-dynamic-range-%E2%80%93-fact-or-fiction/

[7] G. McNally, “Digital audio: dynamic range control of digital audio signals”, BBC Report, BBC RD 1983/17.

[8] Analog Devices, *Analog Dialogue*, Volume 1, Number 3, September 1967, Available at http://www.analog.com/ library/analog Dialogue/ cd/vol1n3.pdf#page=1
[9] Texas Instruments Inc., *Operational amplifier OPA627* Available at http://www.ti.com/lit/ds/symlink/opa627. pdf
[10] B. Blesser, "Digitization of Audio", *J. Audio Eng. Soc.*, vol. 26, no. 10, pp. 739-771, October 1978,.
[11] K. Pohlmann, *Principles of Digital Audio*, Fourth Edition, McGraw Hill, 2000
[12] M. Werwein and M. Schick, *Handbuch der Audiotechnik*, Kapitel 17, Wandler, Prozessoren, Systemarchitektur, VDI-Buch, Springer, Berlin and Heidelberg, 1. Auflage, 2008

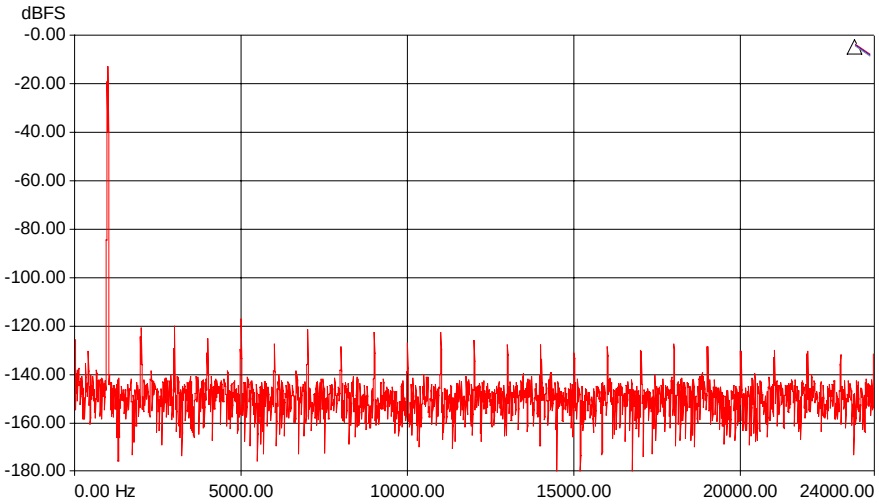

Figure 15: *N=2 dual range adc at output level –13dBFS*

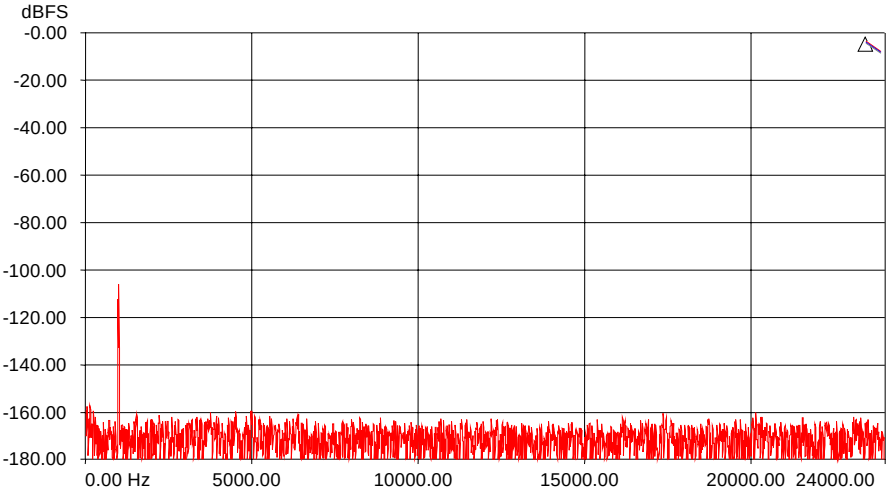

Figure 16: *N=2 dual range adc at output level –103dBFS*